ABSTRACT OF THE DISCLOSURE

~~In a~~ A nonvolatile semiconductor memory device capable of controlling a single memory chip similar to a plurality of memory chips~~, the~~. The memory chip has a plurality of ~~EEPROM~~ Electronically Erasable Programmable Read Only Memory circuits, each of which includes a control circuit for carrying out ~~a writing sequential control and which share~~ sequential writing control and which EEPROM circuits share a data bus. Each of the EEPROM circuits has a ~~chip enable~~ Chip Enable terminal CE and a Ready/Busy terminal R/B, so that data writing processes can be simultaneously carried out in the respective EEPROM circuits in parallel. The activity and inactivity of each of the EEPROM circuits may also be controlled by a logical combination of a master chip enable signal and a chip enable signal of each of the individual EEPROM circuits. A pass or fail result of writing operations may be output or held and accumulated, with the nonvolatile semiconductor memory device having modes of operation in which it is determined whether data may be input to a data buffer by selectively referring to a pass/fail result.